WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit testing system for testing electric characteristics of a plurality of semiconductor integrated circuit devices formed on a semiconductor wafer in the lump, comprising:

a wafer tray for holding said semiconductor wafer;

an interconnect substrate facing said semiconductor wafer held by said wafer tray and having interconnect layers to which a testing voltage is externally input;

a ring-shaped sealing member provided between said wafer tray and said interconnect substrate for forming a sealed space together with said wafer tray and said interconnect substrate;

an elastic sheet held on said interconnect substrate at a periphery thereof;

a plurality of probe terminals provided on said elastic sheet in positions respectively corresponding to external electrodes of said plurality of semiconductor integrated circuit devices and electrically connected to said interconnect layers; and

a plurality of protrusions protruding toward said wafer tray and provided on said elastic sheet for preventing said interconnect substrate from deforming toward said wafer tray when an internal pressure of said sealed space is reduced.

2. The semiconductor integrated circuit testing system

of Claim 1,

wherein said plurality of protrusions are disposed in a region on said elastic sheet where said plurality of probe terminals are distributed relatively sparsely.

3. The semiconductor integrated circuit testing system of Claim 1,

wherein said plurality of protrusions are disposed in a region on said elastic sheet outside a region where said plurality of probe terminals are provided.

4. The semiconductor integrated circuit testing system of Claim 1,

wherein said plurality of protrusions are arranged circumferentially in a region on said elastic sheet corresponding to a periphery of said semiconductor wafer.

5. The semiconductor integrated circuit testing system of Claim 1,

wherein said plurality of probe terminals are composed of electrically connecting isolated patterns provided on a first face of said elastic sheet facing said interconnect substrate and electrically connected to said interconnect layers, and bumps respectively integrated with said electrically connecting isolated patterns and provided on a second face of said elastic sheet facing said wafer tray, and

said plurality of protrusions are composed of dummy isolated patterns provided on the first face of said elastic

sheet, and dummy bumps respectively integrated with said dummy isolated patterns and provided on the second face of said elastic sheet.

6. The semiconductor integrated circuit testing system of Claim 5,

wherein a pressing force applied to all of said dummy isolated patterns when the internal pressure of said sealed space is reduced is approximately 1/3 or more of a pressing force applied to all of said electrically connecting isolated patterns when the internal pressure of said sealed space is reduced.

7. A semiconductor integrated circuit testing method using a testing system including a wafer tray for holding a semiconductor wafer on which a plurality of semiconductor integrated circuit devices respectively having external electrodes are formed; an interconnect substrate having interconnect layers to which a testing voltage is externally input; a ring-shaped sealing member provided between said wafer tray and said interconnect substrate for forming a sealed space together with said wafer tray and said interconnect substrate; an elastic sheet held on said interconnect substrate at a periphery thereof; a plurality of probe terminals provided on said elastic sheet in positions respectively corresponding to said external electrodes of said plurality of semiconductor integrated circuit devices

and electrically connected to said interconnect layers; and a plurality of protrusions protruding toward said wafer tray and provided on said elastic sheet,

the method comprising the steps of:

holding said semiconductor wafer on said wafer tray with said external electrodes of said plurality of semiconductor integrated circuit devices respectively facing said plurality of probe terminals provided on said elastic sheet;

forming said sealed space with said wafer tray, said ring-shaped sealing member and said interconnect substrate by making said wafer tray holding said semiconductor wafer and said interconnect substrate come close to each other;

reducing an internal pressure of said sealed space for bringing said plurality of probe terminals into contact with said external electrodes respectively facing said plurality of probe terminals; and

testing electric characteristics of said plurality of semiconductor integrated circuit devices in the lump by applying the testing voltage to said external electrodes in contact with said plurality of probe terminals through said interconnect layers and said plurality of probe terminals,

wherein the step of reducing the internal pressure of said sealed space includes a sub-step of preventing said interconnect substrate from deforming toward said wafer tray

by bringing said plurality of protrusions into contact with said semiconductor wafer held on said wafer tray.

8. The semiconductor integrated circuit testing method of Claim 7,

wherein said plurality of protrusions are disposed in a region on said elastic sheet where said plurality of probe terminals are distributed relatively sparsely.

9. The semiconductor integrated circuit testing method of Claim 7,

wherein said plurality of protrusions are disposed in a region on said elastic sheet outside a region where said plurality of probe terminals are provided.

10. The semiconductor integrated circuit testing method of Claim 7,

wherein said plurality of protrusions are arranged circumferentially in a region on said elastic sheet corresponding to a periphery of said semiconductor wafer.

11. The semiconductor integrated circuit testing method of Claim 7,

wherein said plurality of probe terminals are composed of electrically connecting isolated patterns provided on a first face of said elastic sheet facing said interconnect substrate and electrically connected to said interconnect layers, and bumps respectively integrated with said electrically connecting isolated patterns and provided on a

second face of said elastic sheet facing said wafer tray, and

said plurality of protrusions are composed of dummy isolated patterns provided on the first face of said elastic sheet, and dummy bumps respectively integrated with said dummy isolated patterns and provided on the second face of said elastic sheet.

12. The semiconductor integrated circuit testing method of Claim 7,

wherein a pressing force applied to all of said dummy isolated patterns when the internal pressure of said sealed space is reduced is approximately 1/3 or more of a pressing force applied to all of said electrically connecting isolated patterns when the internal pressure of said sealed space is reduced.